

Remote Access Digital Combination Circuit Experiment Set Based on FPGA Using IC Package Simulation

Kaung Myat Naing, Panee Noiying and Narissorn Sangkanong

Department of Teacher Training in Electrical Engineering, King Mongkut's University of Technology North Bangkok, 1518, Pracharat 1 Road, Wongsawang, Bangsue, Bangkok 10800

Email: tukaungmyatnaing@gmail.com, drpanee@gmail.com, narissorn.s@fte.kmutnb.ac.th

Abstract- This research aims to establish the remote access digital combination circuit experiment set based on FPGA using IC (Integrated Circuit) package simulation to solve the problem of insufficient laboratory equipment and budget and to apply the set in digital electronics lab at Technological University (Dawei), Myanmar. It consists of two parts. The first part is the IC package simulation that is created by Verilog Hardware Description Language (VHDL) in Quartus II software. The second part is the remote access digital circuit experiment set that composes of client application and lab server application with digital circuit experiment module. These two applications are connected together by local area network (LAN) to become the remote access lab. Moreover, Web Camera are setting-up over the experiment module of lab server application to show the result. Finally, the system is tested by student who studied digital combinational logic course from TU(Dawei) and evaluated in terms of usability, functionality and performance by students and experts. The result represented that the experts rated at high satisfaction level and the students rated at very high satisfaction level.

Keywords- Digital Circuit, FPGA, Remote Access LAB, VHDL

I. INTRODUCTION

The digital electronics is one of the most critical course for Electronic Engineering curriculum at TU(Dawei), Myanmar. In curriculum, digital electronics subject is the second-year course of undergraduate students and it has two semesters (Digital Electronics I and II). According to Electronic Engineering Curriculum, Digital Electronics I (EcE-21021) is a 2.5 credit-points course (2-periods lecture and one-period lab per week). It has been described as the combinational logic course because it took the chapter 1 to 6 from the reference book, "Digital Fundamentals (11th Edition) by Thomas L. Floyd" [1]. This reference book was changed in the previous year (2015-2016 Academic year) instead of "Digital Fundamentals (8th Edition) by Thomas L. Floyd." In this point, the researcher wants to present about engineering education system in Myanmar. Since the board of electronic engineering education assigned the entire curriculum, the same format education system is used in all of Technological University except Yangon Technological University (YTU), Mandalay Technological University (MTU) and Technological University (Yadanarpon Cyber City). Moreover, the ministry of education manages to all of the University such as courses, lab equipment, budgets, student's enrollment and so on.

Therefore, digital electronics course is the same as other Technological University and its course lab equipment received proportionally from ministry of education. Sometimes, the lab equipment was not enough for students experiment.

In the past, the digital electronics lab has been used 74xx family ICs and other electronics devices such as project board, various colored wires, LEDs, resistors and so on. When we used the original ICs, we faced the problems such as IC broken and lab equipment shortages. As mentioned above, TU(Dawei) is non-autonomous university and we do not have the enough budget to buy the needed ICs and other electronic devices. To overcome the above problems, we needed the cost effective and efficient lab environment and the experiment set.

In this research, we design the remote access experiment set based on FPGA and use VHDL to create IC package simulation for solving the above problems. Finally, we test and evaluate this experiment set by students and experts.

II. OTHER RELATED WORKS

A. Previous Studies

Many techniques have been introduced for remote access laboratory [2]-[3]. These researches describe remote access based on FPGA (Field Programmable Gate Array) lab system in both its construction and it is important to engineering education. For digital electronics lab, the FPGA based remote access lab is suitable and useable because FPGA is popular and widely used in digital electronics design and laboratory. Also, FPGA can reprogrammable and make more testing. Moreover, the design of digital electronics lab using FPGA has some advantages such as fault-tolerant, reusability of code, flexibility, easy interface with peripherals, reduce size and accurate simulation [4]. On the other hand, this remote access lab can be used to one subject of the fourth-year course, namely "Digital Design with HDL."

After creating the remote access lab, we are required the digital circuit experiment set for the teaching process which are covered to the teaching topics. Reference [5] describes the design of low cost, reduce damage FPGA-based experiment set which are used in training system for

combinational logic design course. Moreover, the FPGA-based development boards are useful for several classes as the student lab equipment [6]. Also, it can reduce the cost of equipment and can improve the student learning skills. In some reference, researcher compares their student academic performance result in both the 74xx family ICs-based lab-experiments and the FPGA-based lab-experiments [7]. The researcher in reference [7] was mentioned the 74xx family ICs-based lab-experiments is better because the student has a problem in Verilog programming language of FPGA-based lab-experiment. But students are needed to familiar with the real programmable logic devices (PLDs) because of the used in practical industry designs. Therefore, we design the lab with IC package simulation for solving this research problem.

When the experiment set based on FPGA used for the lab equipment, the Quartus II software plays as the important roles. This software can handle with Verilog HDL (hardware description language). In fact, the second-year students do not have good programming skills because they will start to study the programming language at that year. Therefore, this research will create and use the ICs package simulation from “Block Diagram/Schematic design files” of Quartus II software. In the FPGA-based remote access lab, we needed the computers to run the software and compile to FPGA board. To be convenient all of the students, we will use the computer room from TU (Dawei). To summarize the above facts, this FPGA based remote access lab is not only suitable for combinational logic course but also be reduced the costs of lab equipment.

B. Quartus II and DE 10 Nano Development Board

In this research, Quartus II Web Edition v13.1 software is used for designing of digital combination circuit and DE 10 Nano development board is suitable for experiment set.

In FPGA designs, the flow is as follows [2], and often with many feedbacks and modifications:

1. Project description and specification.
2. Design entry through schematic capture or Hardware Description Language.
3. Functional simulation of the design.
4. Design synthesis.
5. Design implementation, and post place and route simulation.
6. FPGA hardware reconfiguration.

Design verified: testing and debugging.

Stages 1 through 5 do not require hardware access. The needed software tools are available free of cost from Altera. Quartus II by Altera is a PLD Design Software which is suitable for high-density FPGA designs, low-cost FPGA designs, and Complex Programmable Logic Devices (CPLD) designs. The Quartus II provides functionality for verifying VHDL code and schematic diagram, synthesizing hardware and generating reports about the analysis and synthesis.

TABLE I Family and Device Setting

Family	Cyclone V
Package	UFPGA
Pin Count	672
Speed Grade	7

Table I showed that FPGA board family and device setting that are used in the creation of the software file in Quartus II.

Stage 6 and 7 require the hardware device. In this research, DE 10 Nano Development Board (FPGA board) is used as a demonstration tool for experiment set. Its FPGA is Cyclone® V SE 5CSEBA6U23I7 with EPCS128 serial configuration device. Since it has 110k logic elements, many types of ICs simulation can create in this device. This board can draw power and program via its onboard USB blaster II, which allows user data transfer from the PCs.

III. DESIGN OF IC PACKAGE SIMULATION

In this section, the design of IC package simulation will be discussed. The package is designed with an objective to assist experiment units of digital combinational logic course.

A. Experiment Units of Digital Combinational Logic Course for Experiment Set

The experiment units are selected from digital combinational logic course which are assigned from the reference book, “Digital Fundamentals (11th Edition) by Thomas L. Floyd” [1]. Three experiment units and one manual are contained in this part as follows:

1. Introduction to basic logic gates
2. Binary adder circuits
 - 2.1 Half and full adder circuit
 - 2.2 2-bits and 4-bits parallel binary adder circuit
3. Decoder circuit
 - 3.1 Basic binary decoder circuit

3.2 4-bits decoder circuit

4. Manual of Quartus II Software, DE10-Nano development board and Lab Modules

B. Creating IC Package Simulation

Quartus II can use logic symbols for block diagram/schematic design file and VHDL for programming language design file. The experiment units use IC simulation symbols to avoid the complex of digital combination circuit design and use as real IC function. However, Quartus II does not contain the IC simulation symbol and it has only logic gate. The IC simulation symbols are created by using VHDL in Quartus II. The pin assignment of IC simulation symbol is the same as IC datasheet that show in Fig. 1.

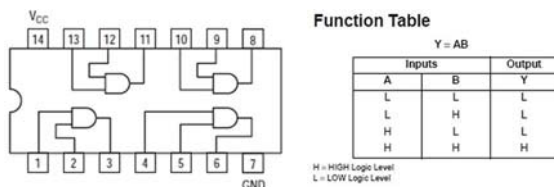


Fig 1. The example of pin assignment and truth table (IC 7408 AND Gate)

The required IC simulation symbols are created in this research as the simulation IC package in Quatus II. IC package simulation includes 26 types of IC that are assigned from digital combinational logic course of the reference book. For designing experiment on Block Diagram/Schematic file of Quartus II, the IC package file is added to the project library. Then the IC can select from this IC package file by does not want to understand the VHDL programming language. Fig. 2 shows the design flow for IC package creation.

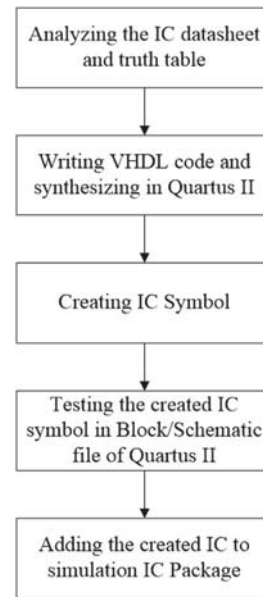
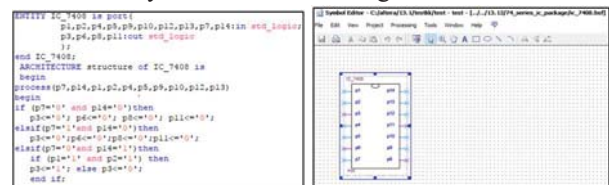
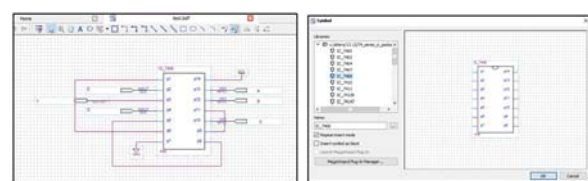


Figure 2. Design steps for simulation IC package creation

At the beginning step, the functional statement of each IC has to be analyzed from IC datasheet. The second step is the design entry, which includes the VHDL code writing in Quartus II software Environment. And then the VHDL code has to be compiled/simulated for the functionality of the design. Fig. 3(a) is as an example of some VHDL code for 7408 IC. The third step is the creation of IC symbol. In this step, the code will be synthesized for creating the IC symbols and the pins of IC symbol are rearranged as the real IC pins as shown in Fig. 3(b). The fourth step is an implementation for testing the created IC with the full function as shown in Fig. 3(c). Finally, the created IC is added to 74 series IC package folder. And then student can select the IC symbol as shown in Fig.



(a) Some VHDL code for 7408 IC (b) Rearranging the created IC pin



(c) Testing the created IC (d) Selecting the IC from IC package

Figure 3. Design procedure of simulation IC package

IV. THE ARCHITECTURE OF REMOTE ACCESS LABORATORY SYSTEM AND EVALUATION

In this section, the architecture of remote access laboratory system and the evaluation method will be discussed. One experiment set of remote access laboratory system is shown in Fig. 4. In this research design, the local area network (LAN) is used instead of the internet because TU(Dawei) does not have internet and Wi-Fi network. The remote access laboratory can solve a problem for lacking of equipment in laboratory environment because one system has 4 student groups (8 students). Moreover, this remote laboratory experiment result is shown by Web Camera.

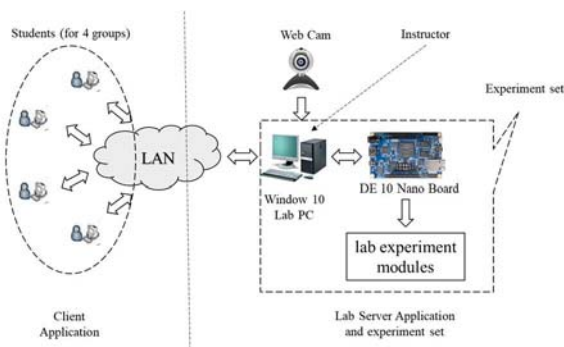


Figure 4. The system architecture of the remote access laboratory for one experimental set

The remote access laboratory composes of:

- Clients application: it contains student group's PC with window 7 (64-bit operating system) and above.
- Lab server application: it contains one lab server PC as similar to student PC.
- The experiment set: it contains FPGA board and lab module. It is connected with lab server application.
- The local area network (LAN): it is used to connect between client application and lab server application by using wire or wireless. One Dual band access point router which contains LAN 4 ports is used for this network.
- Software: Quartus II is used for digital combination circuit design and TeamViewer is used for connecting between client and server via LAN.
- Other supported equipment: 1920x1080 pixels OKER Full HD 386 Web Camera is used for showing experiment results.

For one remote access experiment set, it consists of 5 PCs (4 for student groups and 1 for lab server). So, this

system used 2 experiment sets for 8 student groups. This system can be divided into two applications: client application and lab server application.

This section consists of four parts:

- Client application,
- Lab server application and lab module experiment set,
- The process of remote access digital combination circuit experiment set, and
- Evaluation of satisfaction level on remote access digital combination circuit experiment set.

These four parts are described in the following statements.

A. The Client Application

The client application is aimed for student who learning the experiment units. The sequences of client application are described in Fig. 5.

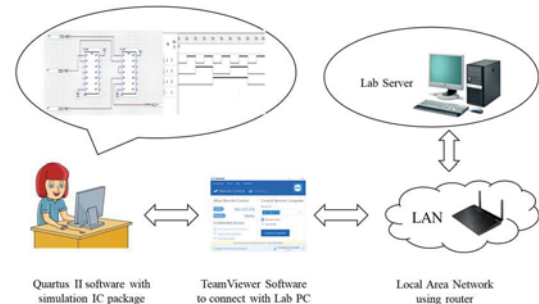


Figure 5. Sequence steps of client application

Before starting this sequence, client PC is required to install Quartus II, TeamViewer and IC package simulation file. According to this sequence, students are locally required to accomplish all stages of the experiment design such as schematic/block diagram, functional simulation, input/output pin assignments, implementation and so on. All of student group can be used simultaneously. The client PCs connect to lab server by LAN network and TeamViewer software.

B. Lab Server Application and Lab Module Experiment Set

Lab server application is responsible for queuing students request. Fig. 6 represents the sequence of lab server application.

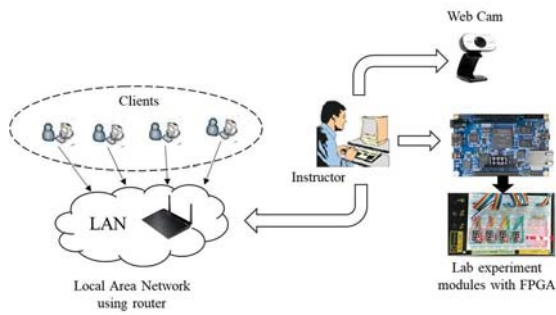


Figure 6. The lab server application

The lab server PC is also required to install Web Camera, Quartus II and TeamViewer. The lab server PC is connected with LAN. The lab server PC is controlled to manage the clients by the instructor with TeamViewer software. Moreover, the lab PC is also connected to the DE 10 Nano development board which is connected with the lab experiment modules.

In the design of lab experiment module, it consists of two modules: LED module and 7-segment module. These lab modules are aimed to cover the experiment unit of the digital combinational logic course. The LED module is designed with eight LED. The 7-segment module is designed with four 7-segments. Each module is connected to the General-purpose input/output (GPIO) port of FPGA board with the connecting wire.

C. The Process of Remote Access Digital Combination Circuit Experiment Set

The process of remote access lab will be described in this section. The flow chat of the remote lab system is shown in Fig. 7.

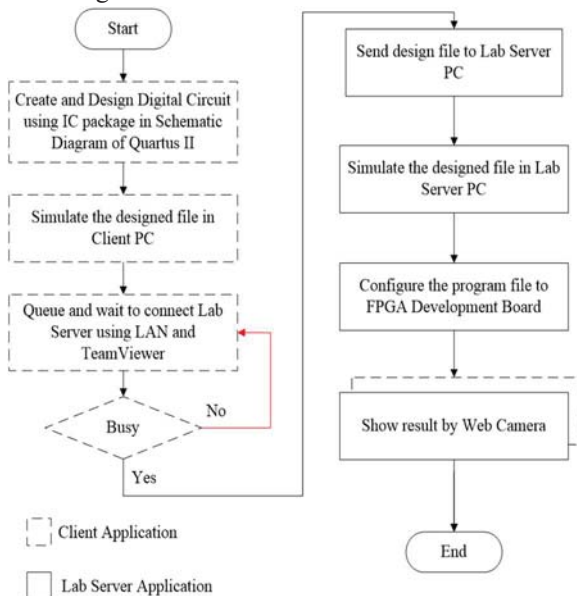


Figure 7. Flow chart for remote access lab system

In this system, the students are created and designed digital circuit from the experiment sheets using IC package

simulation in block/schematic diagram design file of Quartus II. And then the students simulate the design file in their PC from the side of client application. And then they can remotely login to the lab server PC with TeamViewer software. Since the users are limited to connect the lab server PC in this system, the students are queued and waited to connect lab server PC over the LAN network. The instructor at lab server side manages to controls the client PC by TeamViewer software. If the system is busy, the students will not control the lab server PC. On the contrary, if it is not busy, the student will be able to connect to lab server PC and access to remote access lab. Each student group has a limited time (approximately 15 minutes per one topic) to send and test their design file. However, it might be extended if other student groups are not waiting. One experiment unit is designed for 3 hours.

After connecting the lab server, the students can send the experiment design file to the lab PC and simulate their file again with the Quartus II and configure the FPGA devices. At that time, the student can remotely test their design file through the lab server PCs. They compile the program file to FPGA board which is connected with the lab experiment modules such as LED module and 7-segment module. Finally, the students and instructor can check their experiment results with the video live streaming via Web Camera. Throughout these processes, the student can work with all of the experiment conveniently.

D. Evaluation of satisfaction level on Remote Access Digital Combination Circuit Experiment Set

This section describes the evaluation method of satisfaction level on the remote access digital circuit combination experiment set based on FPGA using IC package simulation by students and experts. It was separated into two parts. In the first part, the created remote access experiment set was using with the experiment units by 16 students who learned the digital electronics course at TU(Dawei). And then the students evaluated their satisfaction level upon the remote access experiment set. In the second part, the three experts (TU(Dawei) and KMUTNB) who have been involving or teaching a combinational logic design course for at least 5 years, were asked to evaluate their satisfaction level upon this remote access experiment set and the experiment units. The satisfaction levels were evaluated via rating scale of questionnaires by regarding of usability, functionality and performance. The rating scale using in the questionnaire is ranged from 1(need improvement) to 5(excellent) in each item.

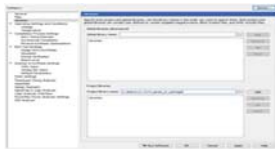
V. RESEARCH RESULTS

The results of the research include three parts: (1) remote access digital combination circuit experiment set

based on FPGA using IC package simulation system, (2) evaluated results of student satisfaction level after using the experiment set and (3) evaluated result of expert satisfaction level for experiment set and experiment units.

A. Remote access digital combination circuit experiment set based on FPGA using IC package simulation system

In this research, FPGA based remote access experiment set was established for EcE-21021 (Digital Electronic I: digital combinational logic courses). Fig. 8 shows the system of the remote access digital combination circuit experiment set based on FPGA using IC package simulation such as installing of IC package file to Quartus II, the setting-up of LAN network, the connecting between lab server PC, FPGA board with lab module and Web Camera. The experiment results can see clearly because the lab module was located under Web Camera.



(a) Inserting of IC package file



(b) Setting-up of LAN network



(c) lab server PC with Web Camera



(d) The experiment lab module

Figure 8. The system of remote access digital combination circuit experiment set based on FPGA using IC package simulation

B. Evaluated results of student satisfaction level after using the experiment set

The satisfaction of remote access digital circuit experiment sets was evaluated by students, as shown in Table II and in Fig. 9.

TABLE II Evaluation of Satisfaction Result for Remote Access Digital Combination Circuit Experiment Set Based on FPGA (Student)

Number of Student = 16

No.	Evaluation items	Appropriate level		
		Average	S.D.	Level
1.	Usability	4.76	0.51	Very High
2.	Functionality	4.77	0.48	Very High
3.	Performance	4.80	0.44	Very High
Total Average		4.78	0.48	Very High



Figure. 9 Testing the remote access experiment set by students

After testing the remote access experiment set, the students rated very high in all of evaluation items upon the using of remote access experiment set. The reason is because they have never used this system before, and it impressed them. The total average satisfaction level of student is 4.78 and standard deviation is 0.48.

C. The Evaluated results of expert satisfaction level after using the experiment set

The satisfaction of remote access digital circuit experiment sets and the experiment units of lab sheet were evaluated by experts, as shown in Table III and in Fig. 10.

TABLE III Evaluation of Satisfaction Result for Remote Access Digital Combination Circuit Experiment Set Based on FPGA (Expert)

Number of Expert = 3

No.	Evaluation items	Appropriate level		
		Average	S.D.	Level
1.	Usability	3.86	0.49	High
2.	Functionality	4.24	0.49	High
3.	Performance	3.71	0.49	High
Total Average		3.94	0.49	High



Figure 10. Evaluating the remote access experiment set and lab sheet by experts

The results from the evaluation revealed that the experts rated their satisfaction at a high level in all of the evaluation items. The total average of the experts' satisfaction level was 3.94 and standard deviation was 0.49. One expert suggested that the fabricated lab module should be used. Meanwhile, another expert suggested to adjust the time for doing experiment because some experiment units could not be finished in time.

VI. CONCLUSION AND DISCUSSION

This paper proposes the application of remote access digital combination circuit experiment set based on FPGA using IC package simulation to solve the problem of insufficient equipment, the complex of digital combination circuit, the programming language and the internet. The IC package simulation and the remote access experiment set were solved the above problems. The IC package simulation can be used as the real IC function similar to data sheet and the remote access lab can be covered to not enough equipment and experiment set. This experiment set has been applied to digital combinational logic courses. Three experiment units and one manual were used for the remote access experiment set. During the study, the remote access experiment set was used by 16 students, and they were then asked to rate their satisfaction level. And then, three experts were also asked to rate their satisfaction level on experiment set and experiment units of lab sheet.

The results showed that students rated at a very high satisfaction level because these students like to design and test their LAB. Moreover, these experiment set can solve not enough lab equipment. And then, the experts rated at a high satisfaction level. They satisfied about system design but it has some problem about managing time when students had practice in LAB. On the other hand, this system can apply to other subjects that have simulation and test with hardware. So, this remote access experiment set is cost effective and efficient lab for digital combinational logic course.

It is obvious that the study can be developed with further works. This experiment set could be improved to support the fourth-year course "Digital Design with HDL" with the programming language. Moreover, the remote access lab could be changed local area network (LAN) to internet when TU(Dawei) campus has a better internet connection. If the remote access lab can be used with the internet, the student will be able to test the experiment set anywhere in the university campus using just their own laptop. Therefore, this remote access digital combination circuit experiment set could be a prototype for further studies.

ACKNOWLEDGMENT

I would like to express my sincere gratitude to Thailand International Cooperation Agency (TICA), Technological University (Dawei) and King Mongkut's University of Technology University North Bangkok (KMUTNB) for supporting my research and my study in Thailand.

REFERENCES

- [1] T. L. Floyd, *Digital Fundamentals*, Eleventh ed.: Pearson, 2015.
- [2] R. Hashemian and J. Riddley, "FPGA e-Lab, a Technique to Remote Access a Laboratory to Design and Test," in *2007 IEEE International Conference on Microelectronic Systems Education (M SE'07)*, 2007, pp. 139-140.
- [3] M. L. Ali, M. H. Rahman, and M. A. N. R. Rahaman, "Development of a remote digital system laboratory," in *2012 15th International Conference on Computer and Information Technology (ICCIT)*, 2012, pp. 575-580.
- [4] I. Petrescu, I.-B. Păvăloiu, and G. Drăgoi, "Digital Logic Introduction Using FPGAs," *Procedia - Social and Behavioral Sciences*, vol. 180, pp. 1507-1513, 5/5/ 2015.
- [5] S. Sothong and P. Chayratsami, "Design of combinational logic training system using FPGA," in *2010 IEEE Frontiers in Education Conference (FIE)*, 2010, pp. F4F-1-F4F-4.
- [6] C. G. Haba, "Using FPGA development boards for multi-course laboratory support," in *2014 IEEE Global Engineering Education Conference (EDUCON)*, 2014, pp. 794-797.
- [7] T. Jamil, "Incorporating FPGA-based labs within digital design course- A middle-eastern experience," in *2015 Science and Information Conference (SAI)*, 2015, pp. 1104-1107.

Kaung Myat Naing received the B.E (Electronics) from Technological University (Mawlamyine), Mon State, Myanmar, in 2011. He is currently a assistance lecturer at Department of Electronic Engineering, Technological University (Dawei), Tanintharyi Division, Myanmar. He is studying M.S.Tech.Ed. (Electrical Engineering) at Department of Teacher Training in Electrical Engineering, Faculty of Technical Education, King Mongkut's University of Technology North Bangkok (KMUTNB), Thailand. His research interests include digital electronics and programmable devices.

Panee Noiying received the B.S. degree in Electrical Engineering from King Mongkut's Institute of Technology North Bangkok (KMITNB), Thailand in 2001, the M.Eng. degree from King Mongkut's Institute of Technology North Bangkok (KMITNB), Thailand in 2006 and the Ph.D. degree from University of Lorraine, Lorraine, France in 2013. She is currently a lecturer at Department of Teacher Training in Electrical Engineering, Faculty of Technical Education, King Mongkut's University of Technology North Bangkok (KMUTNB), Thailand. Her research interests include control system, power electronic and neural network.

Narissorn Sangkanong received the B.S. degree in Electrical Engineering from King Mongkut's Institute of Technology North Bangkok (KMITNB), Thailand in 1996 and the M.Eng. degree from King Mongkut's Institute of Technology Lardkrabang (KMILT), Thailand in 2003. He is currently a lecturer at Department of Teacher Training in Electrical Engineering, Faculty of Technical Education, King Mongkut's University of Technology North Bangkok (KMUTNB), Thailand. His research interests include programming, data communication and computer network.